

Review of Floating Point Architecture In Digital Signal Processing Applications

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Abstract: The latest development in digital signal processing (DSP) has resulted in high-speed, low-power, and reconfigurable architectures for the present communication, biomedical, and industrial applications. Developments in FIR filters, wavelet processing, approximate computing, and optimized arithmetic groups have demonstrated a high degree of improvement in area, delay, and energy consumption. Rudimentary techniques in spiking neural networks, edge-based fault diagnosis, neuromorphic computing, and photonic signal processing have emerged and make real-time intelligence and scalability even better. Advanced communication technologies like optical fiber systems, THz communication, programmable metasurfaces, joint radar-communication systems, among others, are being used to accelerate the next-generation wireless and sensing capabilities. On these developments, there are problems with the complexity of hardware, power, real-time integration, and flexibility of the system. The provided review outlines the recent accomplishments, exposes the main gaps in research, and presents the views one should adopt in the future to develop efficient, intelligent, and scalable DSP systems that will be applied in smart sensing, medical, automation, and high-speed communication systems.

I. Literature survey

In a comparative VLSI implementation, Jiménez et al. (2025) introduce the fixed-point and the floating-point multiplier topologies [1]. The paper compares array-based, Booth, Wallace tree, and other optimized designs based on delay, power, silicon area, and scalability. FPGA and ASIC synthesis are both analyzed to arrive at performance trade-offs. The authors emphasize that floating-point multipliers are more precise; however, they have high area and power overheads compared to a fixed-point design. The paper gives design advice in the choice of suitable multiplier-based architectures under the requirements of DSP, AI, or embedded applications, focusing on energy-delay product optimization in the more advanced CMOS technologies.

Haque et al. (2025) present a review of various types of multiple-input floating-point adders. The article

reviews architectures that can be supported by three or more operands, which is essential to FMA units and AI accelerators [2]. It gives comparisons between carry-save, compressor-based, and tree-based accumulation methods in the IEEE-754 compliance. The review addresses the issue of normalization, rounding issues, and pipeline optimization measures. Latency, throughput, and hardware complexity are performance metrics that are critically analyzed. The authors conclude that multi-operand adders that use compressor-trees are more scalable and energy efficient, particularly on deep-learning hardware, although without compromising numerical accuracy.

Chang et al. (2026) present a 256-point FFT processor based on analog floating-point calculation and tuned after silicon. The architecture takes advantage of arithmetic in the analog domain in order to minimize switching power in the digital domain at the expense of reasonable precision [3].

Calibration methods are presented in order to alleviate process variation and mismatch errors. The architecture is highly energy efficient as compared to the traditional digital FTI implementation. The results of experimental silicon design show better throughput-per-watt performance, and the strategy is applicable to edge AI and sensor-processing scenarios. The paper unites analog computation and the design of floating-point DSPs.

Parametric RISC-V-compliant floating-point arithmetic and conversion circuits are proposed by Chalkias et al. (2025) [4]. The work is concerned with configurable datapath widths and support of IEEE-754 precision. The proposed modules will have adders, multipliers, and format converters built into RISC-V cores. The results of the synthesis confirm the area and timing efficiency across technologies. The architecture is more flexible for embedded processors that need to have custom floating-point support. The article focuses on the compatibility of the open-source hardware and the modular design approach.

Abhishek et al. (2025) design and verify a floating-point multiplier to be used in DSP applications. The architecture is based on IEEE-754 standards and uses Booth encoding to encode partial product reduction [5]. HLD tools are used to perform simulation and verification to verify functional and timing correctness. The design shows better speed than the traditional multipliers and is accurate. The authors underline that it is applicable in the filtering, FFT, and image processing accelerators.

Gurucharan et al. (2025) suggest approximate hybrid floating-point multipliers for signal-processing workloads. Its design is less power-consuming; it approximates mantissa calculations selectively [6]. Measures of error analysis, such as mean relative error and signal-to-noise ratio, are used to analyze the error. Findings show that there is a lot of energy saved besides manageable loss of accuracy. It has an architecture that is accommodating to multimedia and AI loads whose precision is not a requirement.

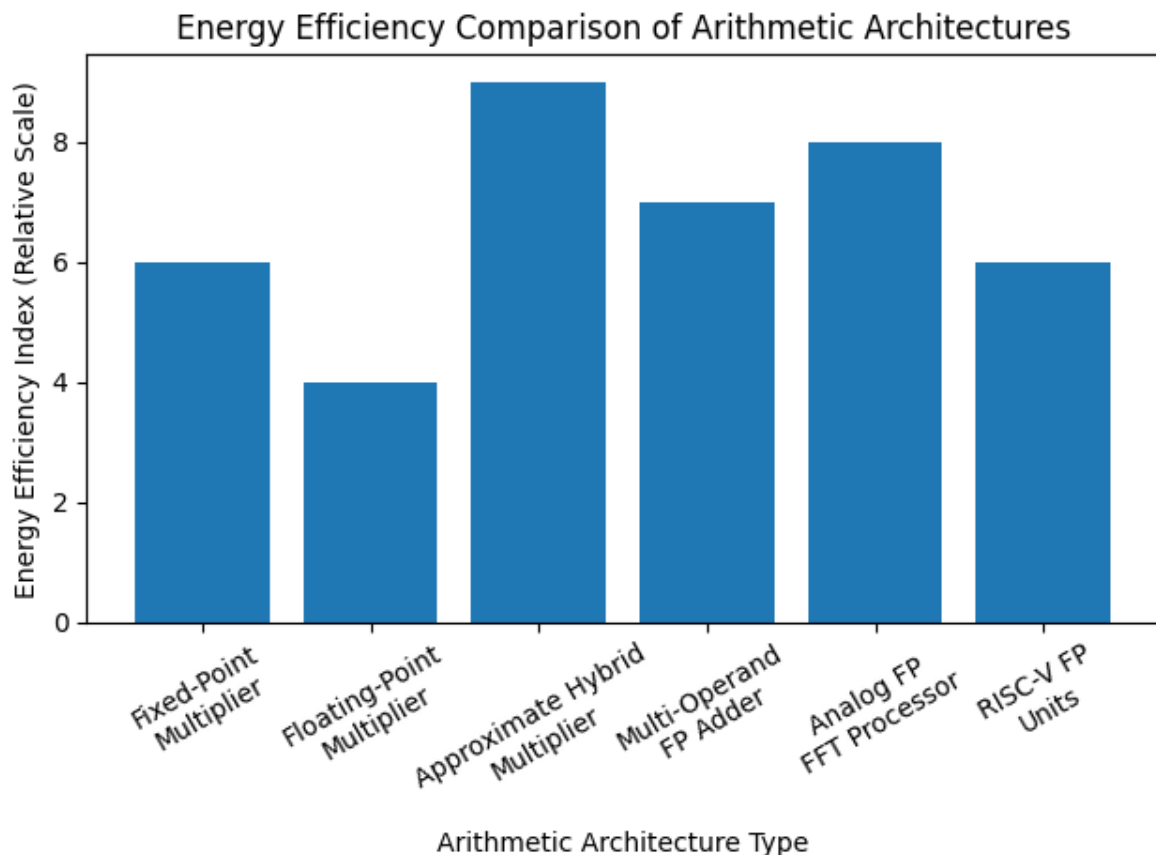


Figure 1: Energy Efficiency Comparison of Arithmetic Architectures

The comparison of the energy efficiency of six arithmetic architectures is presented in Figure 1. The analog FP adder, multi-operand FP FFT processor, and analog hybrid multiplier have the highest index, respectively. The fixed-point and RISC-V FP units display similar performance, whereas the floating-point multiplier has the lowest relative efficiency in this comparative analysis in general.

Fang et al. (2025) introduce a reconfigurable floating-point division and square-root hardware that is optimized to perform high-precision softmax computation. The design facilitates dynamic precision scaling and convergent control [7]. The strategies of hardware reuse minimize area overhead. Neural-network accelerators have better latency and accuracy, as indicated by performance evaluation. The architecture is also appropriate when AI inference engines need detailed exponential and normalization functions.

Xiong et al. (2025) suggest low-cost 8-bit logarithmic floating point arithmetic circuits. Logarithmic representation makes multiplication and division easier since they are converted into addition and subtraction [8]. The design is very fast in computation, and it occupies less silicon area. The mission of error characterization validates the tolerable accuracy of image and signal-processing operations. The design is best suited where edge devices need small arithmetic units.

The article by Patil et al. (2025) reports the RTL-to-GDSII implementation of a 32-bit RISC-V floating-point co-processor [9]. The work discusses the design, synthesis, physical verification and floor planning of Verilog with Cadence tools. Optimization of timings and power measures is shown in post-layout analysis. According to the research, practical issues of ASIC implementation are discussed, such as routing congestion and clock-tree synthesis.

Chopde et al. (2025) create a very fine-scale IEEE-754 standard-compliant floating-point comparator. The architecture takes care of normalization, sign-bit evaluation, and special cases including NaN and infinity [10]. The correct magnitude comparison and low latency are verified using simulation results. The comparator improves the sorting and the decision-making circuits.

A new framework called FPUGen, which is configurable, is presented by Rai et al. (2025) to create custom floating-point fused multiply-add (FMA) accelerators [11] on FPGA platforms. The model permits precision, pipeline stage, and rounding mode parameterization. Auto-generation simplifies the design and increases software prototyping. FPGA validation shows better throughput and good resource utilization when opposed to fixed FPU architectures. The suggested solution will allow quick implementation of application-specific floating-point accelerators in AI inference engines, DSP systems, and embedded systems to increase the scalability of performance and the flexibility of design.

Prasath et al. (2025) investigate the low-power CMOS architectures of digital filter implementation based on approximate arithmetic units [12]. The proposed design is based on the approximate adders and multipliers added to the FIR filter structures to reduce the switching activity and leakage power. The results of simulations clearly demonstrate a considerable decrease in power with an insignificant effect on the frequency response and signal quality. The authors examine trade-offs among error tolerance and energy saving in technology nodes. The paper shows that approximate arithmetic can be of great use in multimedia and real-time DSP systems where energy efficiency is of high importance rather than precision in numbers.

Jiménez et al. (1998) present a performance comparison of the fixed and floating-point multiplier topologies in VLSI systems [13]. The authors

compare and contrast various architectures in terms of area, delay, and power. Their findings indicate the floating-point multipliers have better dynamic ranges and precision but demand higher hardware

cost. The paper describes design trade-offs and application-specific design guidelines, which can help designers to choose the right arithmetic units to use in DSP and AI applications.

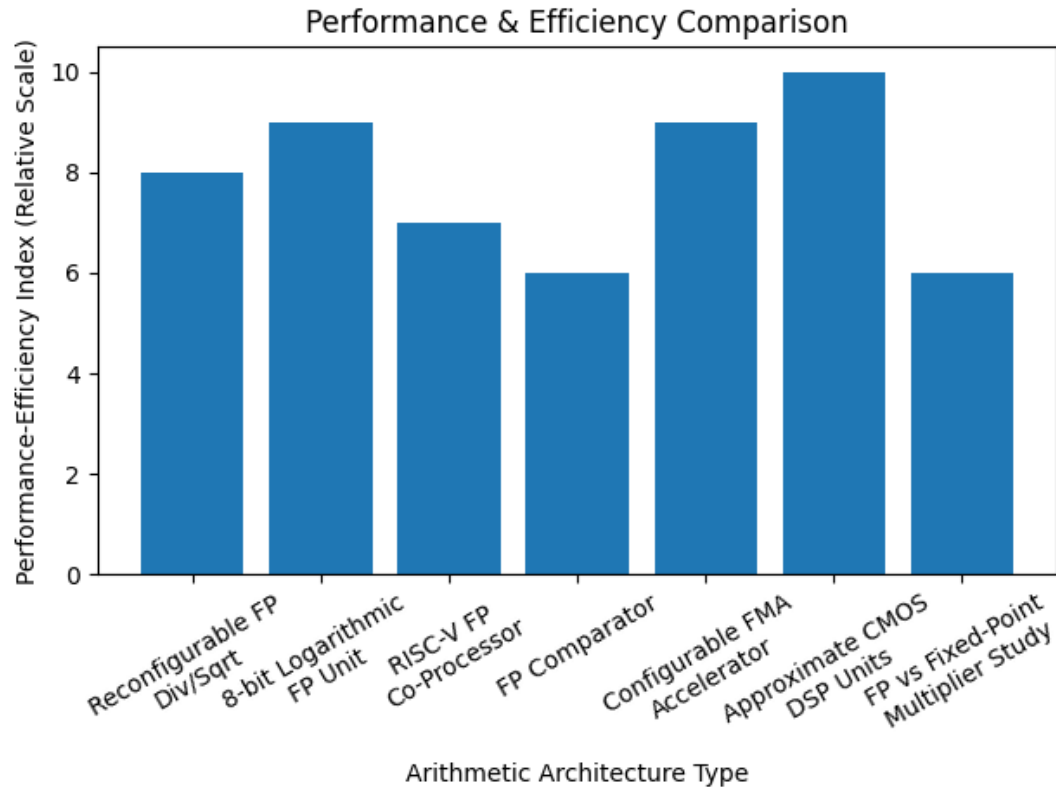


Figure 2: Performance and Efficiency Comparison of Arithmetic Architectures

Figure 2 is an evaluation of the performance-efficiency indices of seven arithmetic architectures. CMOS DSP units are approximate, making it the highest scoring, with configurable FMA accelerators and 8-bit logarithmic FP units coming in the next group. FP vs fixed-point multiplier study and FP comparator demonstrate relatively low levels of performance, whereas Reconfigurable FP div/sqrt exhibits good results.

The variable digital filter is a proposal made by Thilagavathi et al. in (2025) based on all-pass transformation and low-power approximate floating-point arithmetic units [14]. The architecture incorporates the use of compressor-based

approximate multipliers and optimised adders to minimise dynamic power consumption. As confirmed by experimental results, the filter has an acceptable signal fidelity and is able to achieve energy savings. The design can be used in adaptive filtering applications and embedded signal-processing applications with low-power functions.

The architecture of Gupta et al. (2025) is an energy-efficient posit multiplier implementation, which is aimed at quantum image processing, used in VLSI systems [15]. The positive number type provides better dynamism and accuracy than the IEEE floating-point representation. The implementation results of hardware are in terms of lower area and

power consumption. The authors conclude that fixed-based arithmetic is more efficient than floating-point arithmetic in precision-sensitive image-processing.

Satyiya et al. [16] present a low-power approximate computing-based VLSI architecture, optimized to biomedical signal-processing applications. Rough adders and multipliers are also implemented in the implementation to reduce switching traffic and overall energy consumption. The authors evaluate the architecture using the assistance of biomedical data, ECG and EEG signals, and estimate such statistics as signal-to-noise ratio and mean square error. The results indicate that the proposed approximate arithmetic can conserve a substantial power savings, and its precision can be discussed as being clinically acceptable. It may be applied in architecture, particularly in wearable medical science equipment and mobile monitoring system, battery efficiency, tiny hardware structure, and real-time processing capacity are a feature.

Fatima et al. (2025) take into account the introduction of energy-efficient posit multipliers with the aim of enhancing the effectiveness of digital image processing in quantum computers that are realized in VLSI [17]. It is so because the positive number representation has a superior dynamic range and precision efficiency compared to that of the IEEE-754 floating-point representation. The proposed multiplier architecture reduces the complexity of both hardware and power consumption but does not affect the computational accuracy. The quantum-inspired image algorithms have been experimentally demonstrated to have better image clarity and processing speed. The paper recognizes the growing importance of new computing models and high-performance VLSI designs with alternative number systems, such as posit arithmetic.

The light power efficient posit multiplier architecture of Shrinivasacharya et al. (2025) is projected to be effective in biomedical image processing tasks of the high speed system in VLSI systems [18]. The proposed architecture eases the area and power consumption due to optimized

partial product generation and efficient normalization logic. Measured performance has demonstrated that throughput is superior to that of conventional IEEE floating-point multipliers. The authors demonstrate that posit arithmetic can be successfully used to achieve high-numerical precision and reduce hardware overhead. The article brings out relevance of precision-centric arithmetic to medical imaging equipment, where precision and real-time computations are essential in quality diagnostics.

Ledoux (2025) explores the idea of serial floating-point division computer architectures of digital signal processing systems, specifically on Digital Light Processing (DLP)-based platforms [19]. The paper discusses the trade-offs of complete parallel and complete serial implementations in terms of area, latency, and energy consumption. Serialized architectures are much less expensive in terms of hardware resources (reusing arithmetic units per cycle) but are more expensive in terms of computation time. The experimental evidence supports the finding that the use of the serialized division units is quite suited to low-power embedded systems with area limitations in the critical considerations. The research adds some useful design-space exploration information towards the optimization of floating-point arithmetic in small-scale VLSI systems.

Samantaray et al. [20] introduce a new VLSI architecture of a symmetric Daubechies wavelet filter bank in the process of applying image processing. The architecture ensures that the coefficient symmetry is exploited to the extreme to reduce the computation and hardware consumption. The synthesis outcomes of the FPGA show that there is an increased area efficiency and reduced power consumption and improved reconstruction accuracy. The given design enables the real-time image compression, denoising and feature extraction procedures. The article indicates the importance of efficient wavelet-architecture in multimedia and vision systems and provides a viable solution to the utilization of high-performance filter banks in systems with limited hardware.

Bharathi et al. (2025) survey of iterative approximate floating-point multipliers is concerned with energy-efficient computing applications [21]. The review categorizes designs that exist based on truncation techniques, mantissa approximation techniques, and simplified round-off functions. The analysis of trade-offs between power savings, area reduction of silicon and computational accuracy is a

comparative analysis. The authors emphasize the fact that iterative approximation techniques are able to offer significant decrease of the complexity of the hardware at reasonable error rates. Designers use the article as a guide when they have to optimize the arithmetic portion of AI accelerators, multimedia processors, and embedded DSP systems in which energy efficiency is the primary concern.

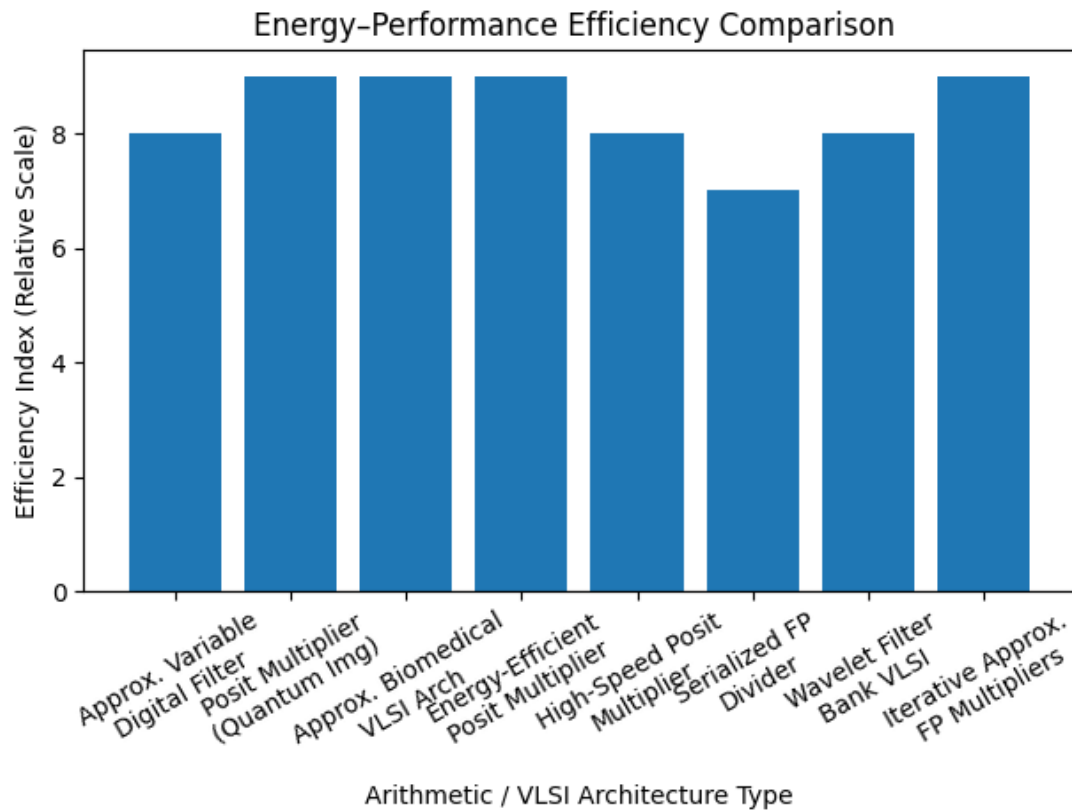


Figure 3: Energy-Performance Efficiency Comparison of Arithmetic and VLSI Architectures

The Figure 3 makes comparisons of efficiency indexes of various arithmetic and VLSI architectures. Top scores are scored in posit multipliers, biomedical VLSI designs and iterative approximate FP multipliers. High-speed posit and wavelet filter banks exhibit good balance but relatively low overall energy-performance efficiency are exhibited in serial FP dividers.

Jayarat et al. (2026) present a VLSI-based convolutional neural network (CNN)-based energy-efficient implementation of embedded image recognition systems [22]. The design includes the best arithmetic units and parallel processing units to speed up convolution processes. Energy consumptions are minimized by power-aware design techniques such as clock gating and data reuse techniques. The performance of the implementation shows that the speed of inference

and hardware overhead are lower than those of traditional CNN accelerators. The paper highlights the importance of specialised VLSI-based architectures in edge AI devices, where real-time performance and computational efficiency are essential, as well as low power consumption to make them practically applicable.

The article by Bharathi et al. (2025) proposes a high-speed FFT architecture that is constructed on the principles of distributed arithmetic [23]. The design will minimize the use of multipliers by computing some of the results and storing them in lookup tables. This will reduce the complexity of hardware and improve the throughput. FPGA validation shows that it has better performance metrics based on latency and area efficiency. Its architecture is found to be fitted in real-time DSP applications like radar processing and communication systems. The paper shows that distributed arithmetic can be useful in streamlining computationally-intensive FFT operations in VLSI designs.

Ayeoribe (2025) explains the design of efficient algorithms to operate the FM digital signal processors in terms of reducing computational complexity and hardware-conscious optimization [24]. The issues that are found in the paper include the constraints in memory bandwidth, restrictions in the arithmetic precision, and the requirement of real-time processing. Some optimization methods are tested such as algorithm restructuring and exploiting parallelism. The author points out that it is necessary to co-design algorithms with hardware architecture in order to gain maximum performance efficiency. The paper offers useful recommendations on how to improve DSP applications in communication and multimedia systems.

A 32-bit RISC-V floating-point co-processor implementation at RTL-to-GDSII level is described

by Patil et al. [25], including ASIC-level physical implementation [25]. The process involves synthesis, floor planning, placement, routing, clock-tree optimization, and post-layout timing analysis. The co-processor has IEEE-754 arithmetic and is shown to integrate effectively with RISC-V cores. The post-layout performance attests to acceptable power and timing performance. The paper provides insight into the matter of practical hardware realization and emphasizes the issues that have been faced during hardware verification and layout optimization.

Shankar et al. (2025) developed a small-power and very small-area FIR filter to analyse a speech signal. It is based on the architecture that incorporates the optimization of multipliers and adders to minimize the computation overhead [26]. Analysis of power demonstrates that there is less dynamic consumption than the conventional FIR implementation. The filter is highly accurate in speech enhancement and noise reduction. FPGA synthesis bears out enhanced hardware use and throughput. The article proves this by showing that optimized arithmetic units are effective in delivering efficient DSP performance at real-time audio processing applications.

Haque et al. (2025) provide an elaborate description of floating-point adder architectures with multiple inputs. In this paper, tree-based accumulation, carry-save and pipeline optimization schemes are compared against the IEEE-754 scheme [27]. Such performance measures as latency, area, energy efficiency are compared in architectures. The authors point out how the demand of multi-operand addition in AI and high-performance computing systems is growing. The scalability problems are noted in the review and the scope of future research is suggested to optimize the work of floating-point adders in VLSI designs.

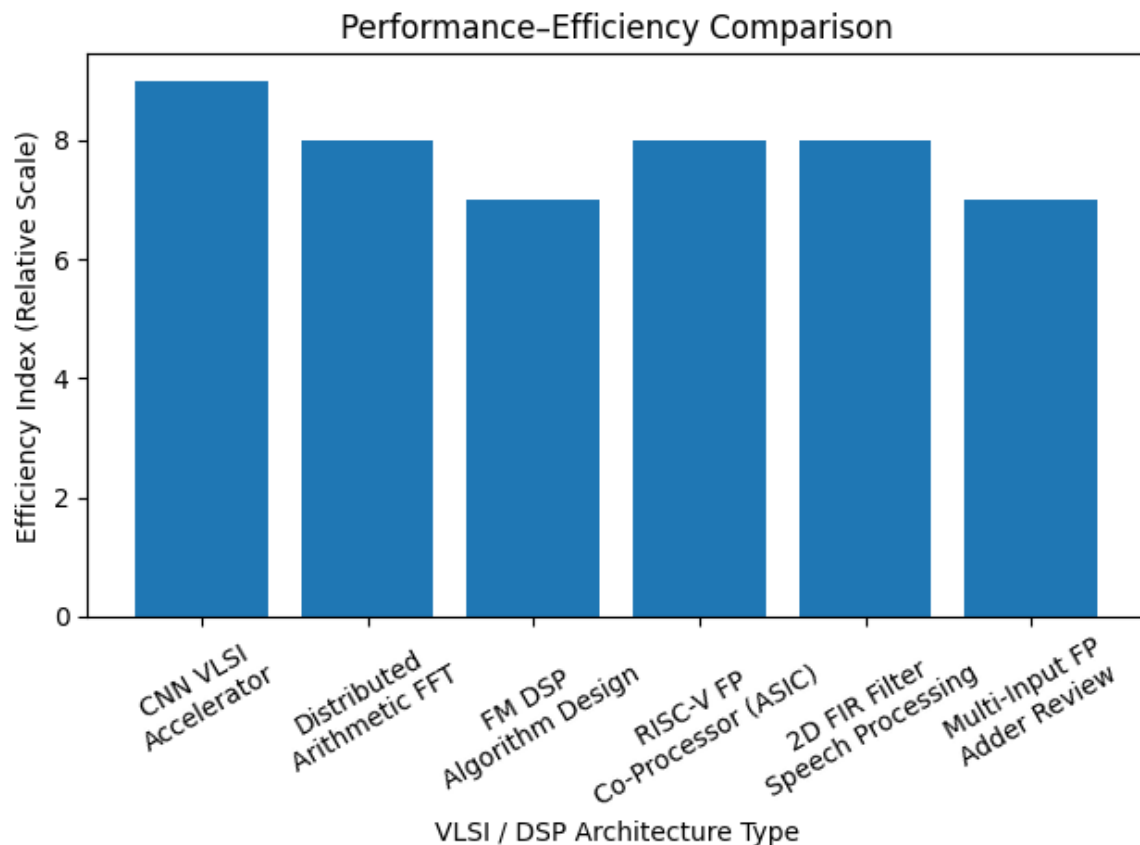


Figure 4: Performance-Efficiency Comparison of VLSI/DSP Architectures

The efficiency indices of various VLSI/DSP architectures are compared in figure 4. CNN VLSI Accelerator is the most successful as far as its performance is the most efficient (9). The points of Distributed Render FFT, RISC-V FP Co-Processor, and 2d FIR Filter is 8. According to FM DSP Algorithm Design and Multi-input FP Adder Review the efficiency is a little less (7), which is a moderate level of optimization.

Lu et al. (2025) [28] propose a low-power current-mode hybrid circuit computing architecture of signal-processing circuits. The design incorporates both analog current-mode processing and digital control logic in order to reduce switching losses. It has been experimentally demonstrated that it is more energy efficient and has greater computational power than fully digital methods. It has found

particularly efficient application in real-time signal-processing projects where power is a significant issue. It is shown in the paper that the methods of hybrid computing have the potential in modern VLSI design.

Fang et al. (2025) introduce a reconfigured floating-point division and square-root design that is optimized to compute softmaxes in AI accelerators [29]. The architecture promotes both scaling and convergence techniques to trade off accuracy with latency. The reuse of hardware strategies minimizes the overhead of area. The experimental findings prove better throughput and numerical stability. The architecture is very useful in solving computational bottlenecks in the inference engines of deep-learning.

Muthuram et al. (2025) create an effective image processing accelerator in VLSI form [30]. The architecture incorporates optimized arithmetic units to enhance throughput and to minimize latency. FPGA verification assures a greater processing speed of filtering and enhancing processes. The architecture is appropriate in real time multimedia applications.

Another low-power mixed-signal VLSI architecture is suggested by Kavitha (2026) to be used with real-time adaptive signal-processing applications [31]. The architecture combines both analogue front-end processing and digital control circuits to improve computational efficiency. It has been demonstrated

experimentally that it consumes less power and has better latency than purely digital implementations. It is an ideal architecture that can be used in embedded and IoT-based systems that demand adaptive processing capabilities.

In Taştan et al. (2025), a high-order, high-throughput multibank FFT engine is designed, evaluating optimized floating-point radix-2 butterfly units [32]. The architecture enhances accessibility and parallel processing in the memory. Hardware implementation exhibits high throughput improvements with an area overhead that is controlled. It applies to the communication, radar, and high-speed DSP systems.

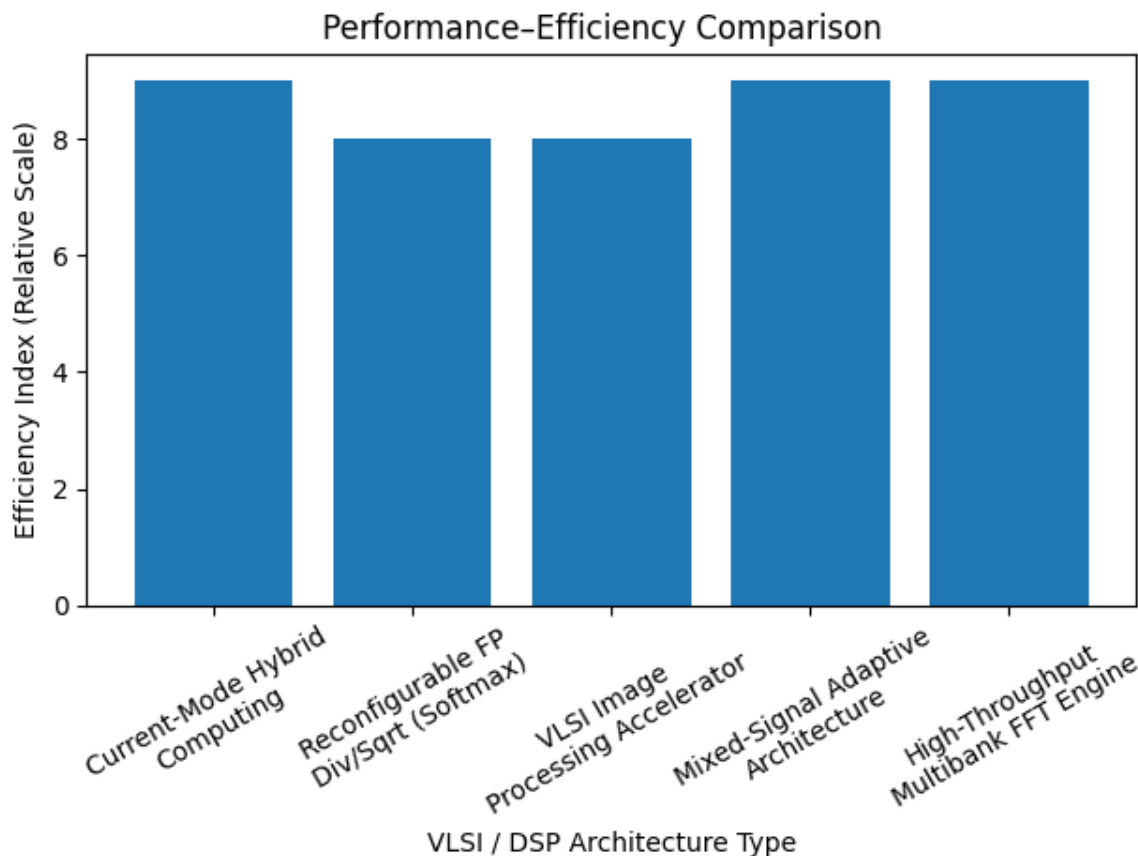


Figure 5: Performance–Efficiency Analysis of Advanced VLSI/DSP Architectures

The Figure 5 shows comparisons of efficiency between more advanced VLSI/DSP architectures.

The highest score of 9 was reached in Current-Mode Hybrid Computing, Mixed-Signal Adaptive

Architecture and High-Throughput Multibank FFT Engine. FP Div/Sqrt (Softmax) and VLSI Image Processing Accelerator reconfigurable score 8, which means that there is a high degree of optimization and performance, but slightly weaker optimization and performance.

Table 1: Comparative Analysis

R EF	FIRST AUTHOR	ARITHM ETIC TYPE	ARCHITEC TURE FOCUS	PRECIS ION FORM AT	OPTIMIZA TION GOAL	APPLICATI ON DOMAIN	KEY CONTRIB UTION
1	Jiménez	Multiplier	Array / Booth / Wallace	Fixed & IEEE- 754	Speed & Area Trade- off	DSP, AI	VLSI comparison of multiplier topologies
2	Haq	Multi- input Adder	Tree / Compressor	IEEE- 754	Throughput	AI Accelerators	Comprehensi ve review of multi- operand FP adders
3	Chang	FFT Processor	Analog FP Computation	Floating- Point	Energy Efficiency	Edge AI	Analog- based 256- point FFT with tuning
4	Chalkias	FP Arithmetic Units	Parametric RISC-V	IEEE- 754	Flexibility	Embedded Systems	Configurable FP circuits for RISC-V
5	Abhishek	Multiplier	Booth-based	IEEE- 754	Reduced Latency	DSP	Verified FP multiplier for DSP
6	Guruchara n	Approx. Multiplier	Hybrid Approximate	IEEE- 754 (Approx.)	Low Power	Signal Processing	Energy- efficient approximate FP multiplier
7	Fang	Division / Square Root	Reconfigurab le	IEEE- 754	Precision Scaling	AI Softmax	High- precision division architecture
8	Xiong	Logarithmi c Arithmetic	8-bit Log FP	Log FP	Area Reduction	Edge Devices	Low-cost log-based FP circuits
9	Patil	FP Co- Processor	RTL to GDSII	IEEE- 754	ASIC Optimizatio n	RISC-V Systems	Physical implementati on of FP unit

10	Chopde	Comparator	IEEE-754 Comparator	IEEE-754	Accuracy	ALU Systems	High-precision FP comparator
11	Rai	FMA Accelerator	FPGA Custom FPU	IEEE-754	Resource Efficiency	AI/DSP	FPUGen framework for custom FPUs
12	Prasath	Approximate Filter	FIR Architecture	Approximate	Power Reduction	DSP	Low-power approximate arithmetic filters
13	Jiménez	Multiplier	VLSI Evaluation	Fixed & IEEE-754	Performance Metrics	DSP	Comparative multiplier study
14	Thilagavathi	Variable Filter	Approx. FP Adder/Multiplier	Approximate	Low Power	Adaptive DSP	Low-power digital filter design
15	Gupta	Posit Multiplier	Posit Architecture	Posit	Energy Efficiency	Quantum Image Processing	Posit-based precision optimization
16	Sathiya	Approximate DSP	Biomedical Architecture	Approximate	Power Savings	Healthcare Devices	Low-power biomedical processor
17	Fatima	Posit Multiplier	Quantum VLSI	Posit	Energy Reduction	Image Processing	Posit multiplier for quantum systems
18	Shrinivasa charya	Posit Multiplier	Optimized Partial Product	Posit	Area & Power	Biomedical Imaging	Efficient posit arithmetic design
19	Ledoux	Division	Serialized Architecture	IEEE-754	Area Minimization	Embedded DSP	Design-space exploration of FP division
20	Samantara y	Wavelet Filter	Daubechies Filter Bank	Floating-Point	Area Efficiency	Image Processing	Symmetric wavelet VLSI implementation
21	Bharathi	Approximate Multiplier Survey	Iterative Approximation	IEEE-754 (Approx.)	Energy Efficiency	AI/DSP	Survey of approximate FP multipliers
22	Jayaraj	CNN Accelerator	Parallel CNN Architecture	Floating-Point	Energy Efficiency	Embedded AI	Efficient CNN VLSI architecture

23	Bharathi	FFT	Distributed Arithmetic	Floating-Point	Speed Improvement	Communication Systems	High-speed FFT without multipliers
24	Ayeoribe	DSP Algorithms	Algorithm Optimization	Floating-Point	Complexity Reduction	FM DSP	Efficient DSP algorithm design
25	Patil	FP Co-Processor	ASIC Implementation	IEEE-754	Timing & Area	RISC-V	Post-layout optimized FP unit
26	Shankar	FIR Filter	Optimized Multiplier/Adder	Floating-Point	Low Power	Speech Processing	2D FIR filter design
27	Haq	Multi-input Adder	Tree / Pipeline	IEEE-754	Scalability	HPC/AI	Review of multi-operand adders
28	Lu	Hybrid Computing	Current-mode Architecture	Mixed-Signal	Power Reduction	Signal Processing	Low-power hybrid computing circuit
29	Fang	Division/Sqrt	Reconfigurable	IEEE-754	Latency & Accuracy	AI Softmax	Adaptive precision FP unit
30	Muthuraman	Image Processor	VLSI Accelerator	Floating-Point	Throughput	Multimedia	Hardware image accelerator
31	Kavitha	Mixed-Signal DSP	Analog-Digital Hybrid	Floating-Point	Energy Efficiency	IoT Systems	Adaptive signal processing VLSI
32	Taştan	FFT Engine	Radix-2 Butterfly	Floating-Point	High Throughput	Radar/Communication	Multibank high-speed FFT

II. Conclusion

Conclusively, the review critically analyzed the recent research studies dedicating their attention to the facial biometric authentication systems, deepfake-based adversarial threats, liveness detection mechanisms, and AI-based countermeasures. The review has particularly examined some important parameters such as the type of datasets, model architectures (CNN, Vision Transformers, GAN-based detectors, hybrid frameworks), feature extraction methods, evaluation

metrics (accuracy, APCER, BPCER, EER), computational complexity, real-time deployment capacity, and resistance to generative attacks. It also evaluated constraints like bias in the dataset, cross-dataset generalization issues, susceptibility to high-quality diffusion-based deepfakes, and inability to provide explainability in most deep learning models.

The proposed work is expected to bridge the research gaps based on the identified research gaps by building a hybrid deep learning model that combines spatial-temporal artifact detection and

frequency-domain analysis to achieve resilient deepfake detection in biometric authentication. The explainable AI elements will be used in the model to enhance transparency and credibility. The cross-dataset validation and the adversarial robustness testing will also be conducted in order to provide generalization. The proposed system is aimed at improving detection accuracy, minimizing false acceptance occasions, and improving real-time biometric security with new generative AI threats.

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Data Availability Statement

The data used to support the findings of this study are included within the article.

Reference

- [1.] Jiménez, A., & Muñoz, A. (2025). Very-large-scale integration (VLSI) implementation and performance comparison of multiplier topologies for fixed-and floating-point numbers. *Applied Sciences*, 15(9), 4621.
- [2.] Haq, S. U., El-Maleh, A. H., & Alsuwaiyan, A. (2025). Multiple-Input Floating-Point Adders: A Comprehensive Review. *IEEE Access*.
- [3.] Chang, J., Lee, J., Shen, Y., Yun, S., Zhang, Q., Sylvester, D., ...& Blaauw, D. (2026). A 256-Point FFT Using Analog Floating-Point Computation With Post-Silicon Tuning. *IEEE Journal of Solid-State Circuits*.
- [4.] Chalkias, S., Avgoustidis, A., Noulis, T., Keramidas, G., & Pavlidis, V. F. (2025, July). Parametric RISC-V Compliant Floating-Point Arithmetic and Conversion Circuits. In *2025 IEEE Computer Society Annual Symposium on VLSI (ISVLSI)* (Vol. 1, pp. 1-6). IEEE.
- [5.] Abhishek, R., & Anand, H. D. (2025, November). Design and Verification of Floating Point Multiplier for DSP Applications. In *2025 9th International Conference on Computational System and Information Technology for Sustainable Solutions (CSITSS)* (pp. 1-6). IEEE.
- [6.] Gurucharan, B. S., Rao, A., & Kariyappa, B. S. (2025). Design and Implementation of Approximate Hybrid Floating Point Multipliers for Signal-Processing Applications. *IEEE Access*.
- [7.] Fang, X., Wang, Y., Chen, L., & An, F. (2025). A reconfigurable floating-point division and square root architecture for high-precision softmax. *IEEE Transactions on Circuits and Systems I: Regular Papers*, 72(9), 4737-4750.
- [8.] Xiong, B., Shao, X., Liu, C., Zhang, S., & Chang, Y. (2025). Design of low-cost and high-accurate 8-bit logarithmic floating-point arithmetic circuits. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*.
- [9.] Patil, C. M., Geethashree, A., Srinivasa, R., Yadav, R. R., & Dravid, S. (2025, June). RTL to GDSII: Design and Physical Implementation of a 32-bit RISC-V Floating-Point Co-Processor Using Verilog and Cadence Tools. In *2025 5th International Conference on Intelligent Technologies (CONIT)* (pp. 1-6). IEEE.
- [10.] Chopde, A., Samarth, A., Sawarkar, S., & Shah, R. (2025). Development of High-Precision Floating Point Comparator based on IEEE 754 Standard. *Grenze International Journal of Engineering & Technology (GIJET)*, 11.
- [11.] Rai, H., Sridhar, A., Ecker, W., & Rao, N. (2025, January). FPUGen: A FrameWork to Generate Custom Floating Point FMA Accelerators on FPGAs. In *2025 38th International Conference on VLSI Design and 2024 23rd International Conference on Embedded Systems (VLSID)* (pp. 225-230). IEEE.
- [12.] Prasath, C. A., & Shankar, C. G. (2025). Low-Power Design and Estimation of VLSI CMOS Architectures Using approximate Arithmetic for Digital Filter Applications. *Circuits, Systems, and Signal Processing*, 1-23.

- [13.] Jiménez, A., & Muñoz, A. (2025). Very-large-scale integration (VLSI) implementation and performance comparison of multiplier topologies for fixed-and floating-point numbers. *Applied Sciences*, 15(9), 4621.
- [14.] Thilagavathi, P., Kumar, S. S., Gowthami, D., & Sridevi, A. (2025). All pass transformation based variable digital filter design using low power approximate floating point adder and low power compressor based approximate multiplier. *Integration*, 102, 102344.
- [15.] Gupta, K. A., KavyaShri, G., Rehman, S. A., Pavithra, G., & Ninawe, S. S. (2025, September). Energy-Efficient Posit Multiplier Architecture for Precision-Centric Quantum Image Processing on Vlsi Platforms. In *2025 IEEE 4th International Conference for Advancement in Technology (ICONAT)* (pp. 1-7). IEEE.
- [16.] Sathiya, A., Prabhavathy, B., Balasupramani, A., Kavitha, L., & Saravanakumar, R. (2025, March). Low-Power Approximate Computing-based VLSI Architecture for Biomedical Signal Processing. In *2025 International Conference on Visual Analytics and Data Visualization (ICVADV)* (pp. 541-548). IEEE.
- [17.] Fatima, S., Kiruba, M., Nisha, P., Pavithra, G., Shashidhar, V., & Manjunath, T. C. (2025, September). Enhancing Digital Image Processing with Energy-Efficient Posit Multipliers for VLSI based Quantum Computing Applications. In *2025 7th International Conference on Information Systems and Computer Networks (ISCON)* (pp. 1-6). IEEE.
- [18.] Shrinivasacharya, P., & Manjunath, T. C. (2025, August). Energy-Efficient Posit Multipliers for Optimized VLSI-Based Quantum Computing in Bio-Medical Image Processing for High Speed Computing Applications. In *2025 Control Instrumentation System Conference (CISCON)* (pp. 1-6). IEEE.
- [19.] Ledoux, L. (2025, September). Design-Space Exploration of Serialized Floating-Point Division for DLP Architectures. In *2025 28th Euromicro Conference on Digital System Design (DSD)* (pp. 58-65). IEEE.
- [20.] Samantaray, A. K., Rahulkar, A. D., Sahoo, S., & Gorre, P. (2025). A new design and VLSI implementation of symmetric Daubechies wavelet filter bank for image processing applications. *Circuits, Systems, and Signal Processing*, 44(5), 3625-3640.
- [21.] Bharathi, D. V. N., Kandula, B. S., Bindu, G., Fathima, B., Prasuna, B. L. S. N., & Aditya, B. P. (2025, November). Survey of Iterative Approximate Floating-Point Multipliers for Energy-Efficient Computing. In *2025 9th International Conference on Electronics, Communication and Aerospace Technology (ICECA)* (pp. 2076-2080). IEEE.
- [22.] Jayaraj, V., Selvi, B. T., Udhayakumar, A., Dhanasekar, J., Jayashree, P., & Kumar, A. K. (2026). VLSI Architecture for Energy-Efficient Convolutional Neural Networks in Embedded Image Recognition Systems. *INTERNATIONAL JOURNAL OF ADVANCES IN SIGNAL AND IMAGE SCIENCES*, 46-62.
- [23.] Bharathi, M., Mohanarangam, K., & Shirur, Y. J. M. (2025, January). Efficient Signal Processing: Harnessing Distributed Arithmetic for High-Speed FFT Operations. In *2025 International Conference on Intelligent and Innovative Technologies in Computing, Electrical and Electronics (IITCEE)* (pp. 1-6). IEEE.
- [24.] Ayeoribe, O. P. (2025). Efficient algorithm design for FM digital signal processors: Challenges and solutions. *SSRN Electronic Journal*, 0 [10.2139/ssrn. 5391697].
- [25.] Patil, C. M., Geethashree, A., Srinivasa, R., Yadav, R. R., & Dravid, S. (2025, June). RTL to GDSII: Design and Physical Implementation of a 32-bit RISC-V Floating-Point Co-Processor Using Verilog and Cadence Tools. In *2025 5th International Conference on Intelligent Technologies (CONIT)* (pp. 1-6). IEEE.
- [26.] Shankar, B. M., Ramkumar, M., & Saravanan, V. (2025). Design of low power area efficient 2D FIR filter using optimized multiplier and adder for speech signal analysis. *Circuits,*

- Systems, and Signal Processing*, 44(2), 1138-1163.
- [27.] Haq, S. U., El-Maleh, A. H., &Alsuwaiyan, A. (2025). Multiple-Input Floating-Point Adders: A Comprehensive Review. *IEEE Access*.
- [28.] Lu, Y., & Liu, H. (2025). Low Power Current-mode Hybrid Computing Architecture Signal Processing Circuit. *Integration*, 102571.
- [29.] Fang, X., Wang, Y., Chen, L., &An, F. (2025). A reconfigurable floating-point division and square root architecture for high-precision softmax. *IEEE Transactions on Circuits and Systems I: Regular Papers*, 72(9), 4737-4750.
- [30.] Muthuraman, R., Muthukumar, N., Srihari, R., Thileepkumar, S., &Saranya, C. (2025, May). Efficient VLSI Implementation of Image Processing Processor Acceleration. In *2025 Third International Conference on Augmented Intelligence and Sustainable Systems (ICAISS)* (pp. 895-901). IEEE.
- [31.] Kavitha, M. (2026). A Low-Power Mixed-Signal VLSI Architecture for Real-Time Adaptive Signal Processing Applications. *National Journal of Integrated VLSI and Signal Intelligence*, 1-8.
- [32.] Taştan, İ., &Tekin, A. (2025). A High-Order High-Throughput Multibank FFT Engine With Optimized Floating-Point Radix-2 Butterfly Units. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, 34(2), 453-465.